REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-16 are pending. Claims 1-16 stand rejected. Claims 6 – 8 have been cancelled. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 112

The Examiner has rejected claims 6-8 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The Examiner has rejected claims 6-8 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The Examiner has stated that

> Claim 6 discloses an apparatus comprising a first input node receiving a first signal that indicates processor utilization has exceeded a first threshold for a first period of time, and a second input node receiving a second signal that indicates processor utilization has fallen below a second threshold for a second period of time. While the specification describes a single processor utilization input into software (Page 8, lines 1-2), the specification does not describe an apparatus with first and second nodes for receiving first and second signals. Nor do the drawing show any signal lines for indicating processor utilization (Fig. 1).

(p. 2-3, Office Action 4/8/04)

Applicants have canceled claims 6 – 8 in response to this rejection.

Rejections Under 35 U.S.C. § 102(e)

Claims 1-9 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,684,341 of Malcolm ("Malcolm"). The Examiner stated that

> As per claim 1, Malcolm discloses a method comprising:
> monitoring processor utilization of a computer system having a processor (Fig. 6, step 600), the processor having a plurality of performance levels. (Col. 7, lines 30-37); and
> automatically transitioning the processor to a higher performance level if it is determined that the processor utilization has remained above a switch-up level for a specified time (Fig. 6, step 608; Col. 8, lines 1-7).
>
> As per claim 9, since Malcolm discloses the method of claim 1, Malcolm discloses the claimed machine-readable medium (Col. 4, lines 10-33).

(p. 3-4, Office Action 4/8/04)

Malcolm states

> The processes of the present invention are performed by processor 202 using computer implemented instructions, which may be located in a memory such as, for example, main memory 204, memory 224, or in one or more peripheral devices 226-228. Furthermore, the processes of the present invention may be implemented with power management 219. Power management 219 may include, for example, registers, Basic Input Output System (BIOS), and tables used to perform power control management on hardware in data processing system 200. Power management functions and processes also may be implemented in an operating system on data processing system 200.
>
> The present invention provides a method, apparatus, and computer implemented instructions for managing power consumption in a data processing system to maximize performance while maintaining power resources sufficient to run the data processing system based on utilization of resources within the data processing system. In the depicted examples, the resource adjustment is made with respect to processor speed for one or more processors located in the data processing system. The resource usage that is monitored for by the mechanism of the present invention is based on the execution or running of applications or programs in the data processing system.

(Col. 4, lines 10-33)

> The process begins by determining the current processor utilization as a percentage (step 600). In these examples, processor utilization is from 0 precent to 100 precent. Next, the current processor speed is determined as a percentage of the range a slowest speed to a fastest speed for the processor (step 602). The processor speed is assigned 0 precent for the slowest speed and 100 precent for the fastest speed.

(Col. 7, lines 30-37)

> The processes may take into account situations like program loading in which a short spike in usage occurs and ignores those spike in making adjustments. Such a mechanism may include mechanisms, such as providing a lag time before adjusting the resources to make sure that the change in usage is not merely a spike or temporary situation.

(Col. 8, lines 1-7)

Applicants respectfully submit that claims 1 and 9 are not anticipated by Malcolm under 35 U.S.C. 102§(e). Claim 1 includes the following limitations:

> A method comprising:
> monitoring processor utilization of a computer system having a processor, the processor having a plurality of performance levels; and
> automatically transitioning the processor to a higher performance level if it is determined that the processor utilization has remained above a switch-up level for a specified time.

(Claim 1) (emphasis added)

Applicants respectfully submit that Malcom does not include the limitation of transitioning to a higher performance level. As defined in the specification, a performance level is an operating frequency and an associated voltage. Automatic transitioning of performance levels allows for adjustment to the processor frequency while maintaining responsiveness. In contrast, Malcolm discloses that a present processor utilization is compared to present processor speed. The processor speed is then increased or decreased based upon this comparison. The comparison of Malcolm does not include comparison of a processor utilization with a processor performance level (speed/voltage).

For these reasons applicants respectfully submit that claim 1 is not anticipated by Malcolm. Given that claims 2 – 5 depend, directly or indirectly, from claim 1, applicants respectfully submit that claims 2 – 5 are, likewise, not anticipated by Malcolm. Further, given that claim 9 includes the limitation of "automatically transitioning the processor to a higher performance level if it is determined that the processor utilization has remained above a switch-up level for a specified time," applicants respectfully submit that claim 9 is not anticipated by

Malcolm. Given that claims 10 - 16 depend, directly or indirectly, from claim 9, applicants respectfully submit that claims 10 – 16 are, likewise, not anticipated by Malcolm.

Rejections Under 35 U.S.C. § 103(a)

Claims 2-5 and 10-16 stand rejected under 35 U.S.C. § 103 as being unpatentable over Malcolm as applied to claims 1 and 9 above, and further in view of U.S. Patent No. 6,574,739 of Kung, et al. ("Kung")

Applicants respectfully submit the combination of Kung does not remedy the deficiency of Malcom as discussed above. Kung discloses external circuitry used to adjust clock frequency or internal operating voltage. Kung does not disclose a performance level of the processor that is specified by a frequency and associated voltage.

It is also respectfully submitted that Malcolm does not teach or suggest a combination with Kung and that Kung does not teach or suggest a combination with Malcolm.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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